New EVG and EVR features in Delay Compensation (DC) capable timing hardware

Spring 2017 EPICS Collaboration Meeting

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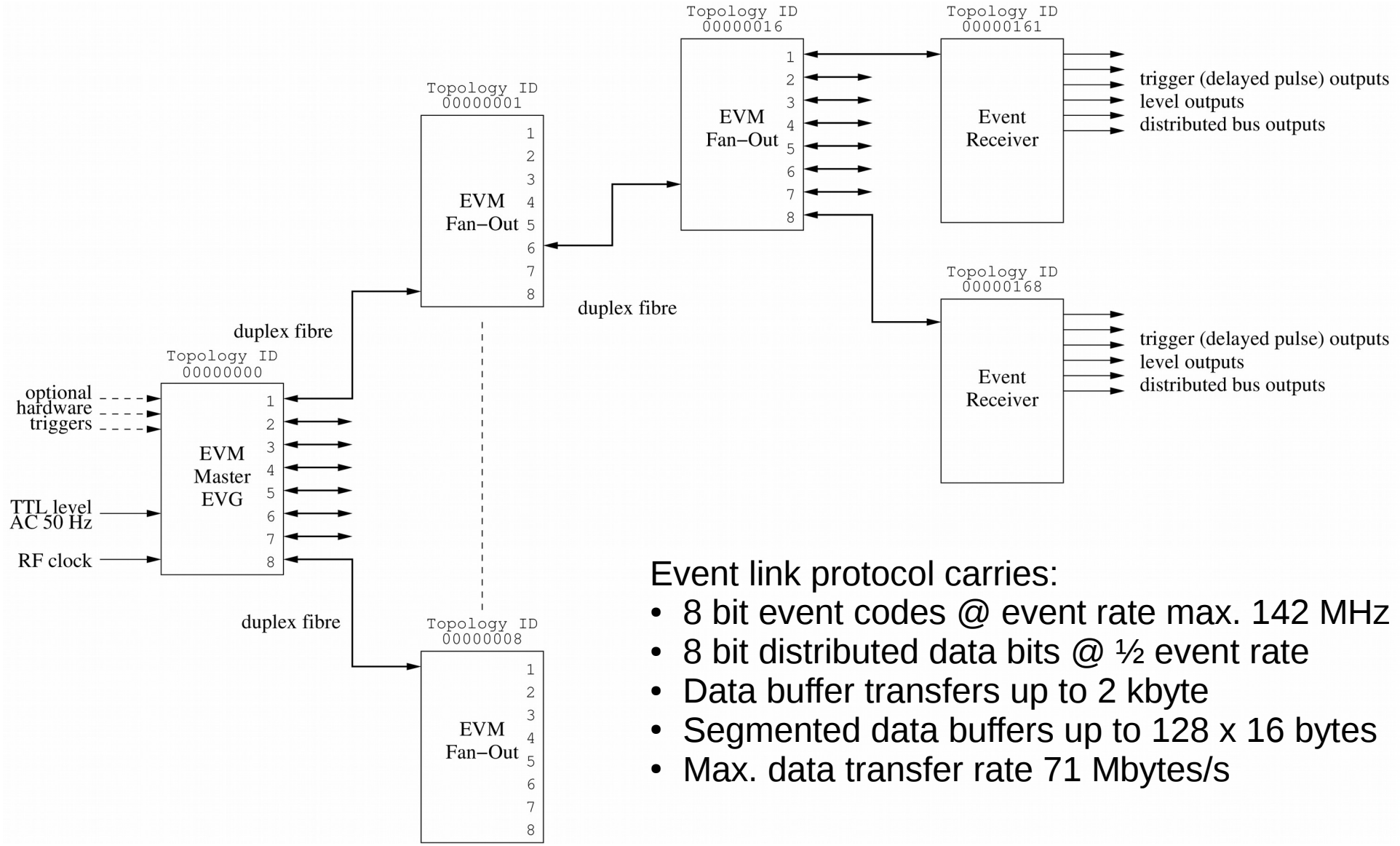
Delay Compensation (DC) Typical System Layout



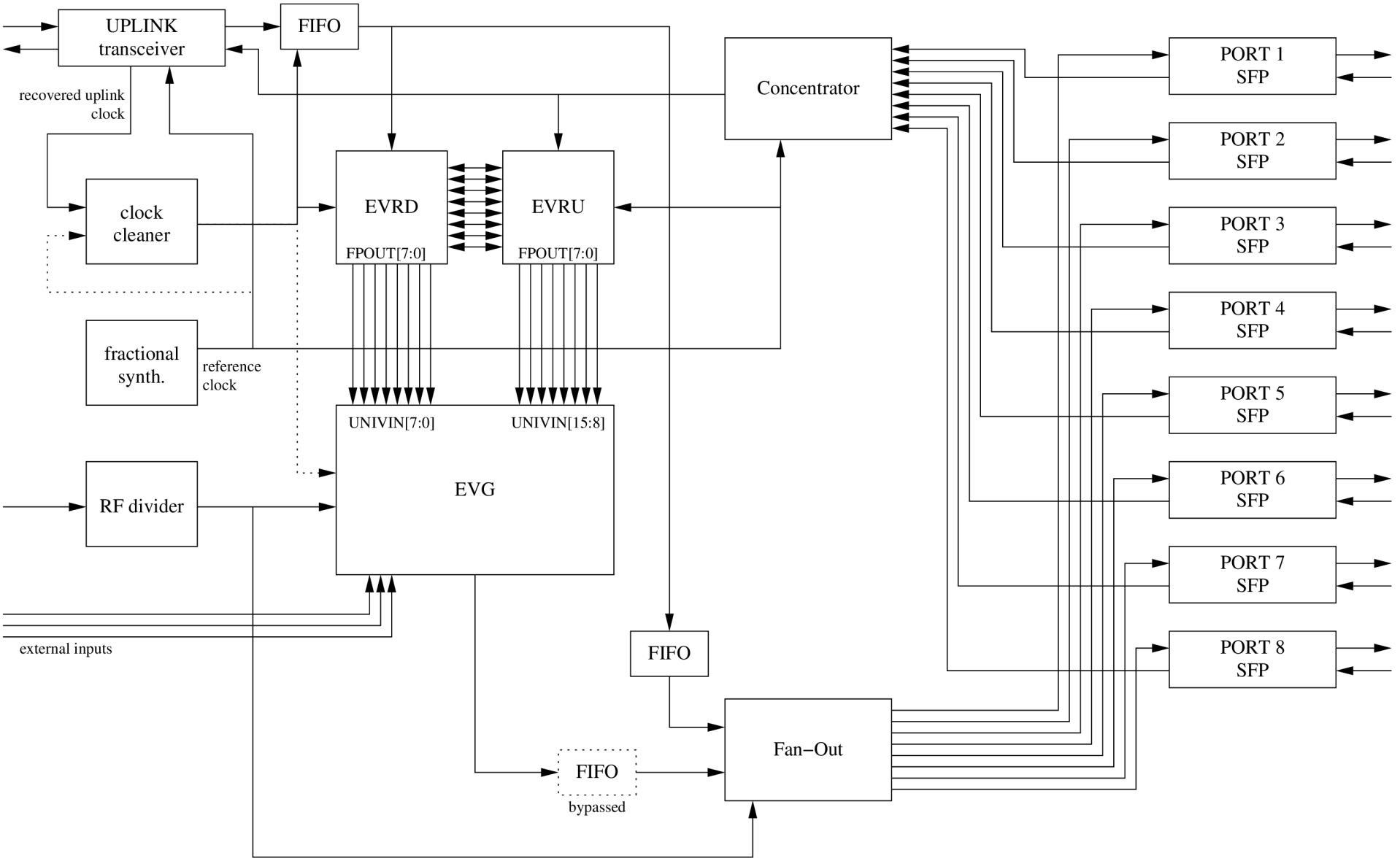
Event link protocol carries:

- 8 bit event codes @ event rate max. 142 MHz
- 8 bit distributed data bits @ ½ event rate
- Data buffer transfers up to 2 kbyte
- Segmented data buffers up to 128 x 16 bytes
- Max. data transfer rate 71 Mbytes/s

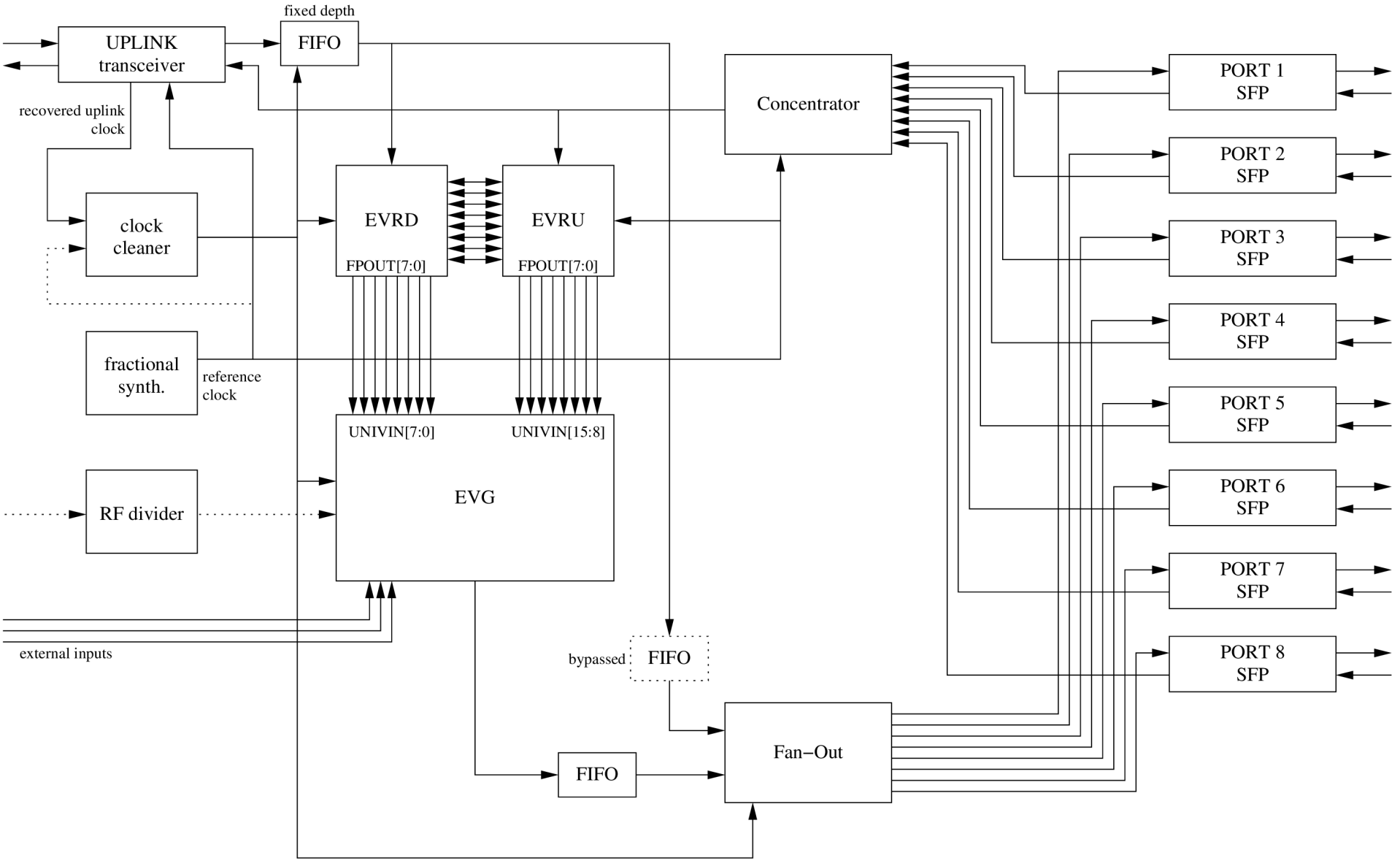
VME-EVM-300

- Event Generator (EVG)
  - 2 sequencers with maskable events
    - Max. 2047 events/sequence
    - 32 bit timestamp
  - 8 multiplexed counters
  - data buffer up to 2k bytes
  - segmented data buffer
    - 127 segments, 16 bytes each
- 8-Way Fan-Out/Concentrator
- Two Event Receivers (EVR)
  - 8 internal pulse outputs
  - one sequencer
- Event rate conversion (with some data buffer related limitations)
- Front panel input phase monitoring/select features
- Distributed bus phase selection
- RF input monitoring

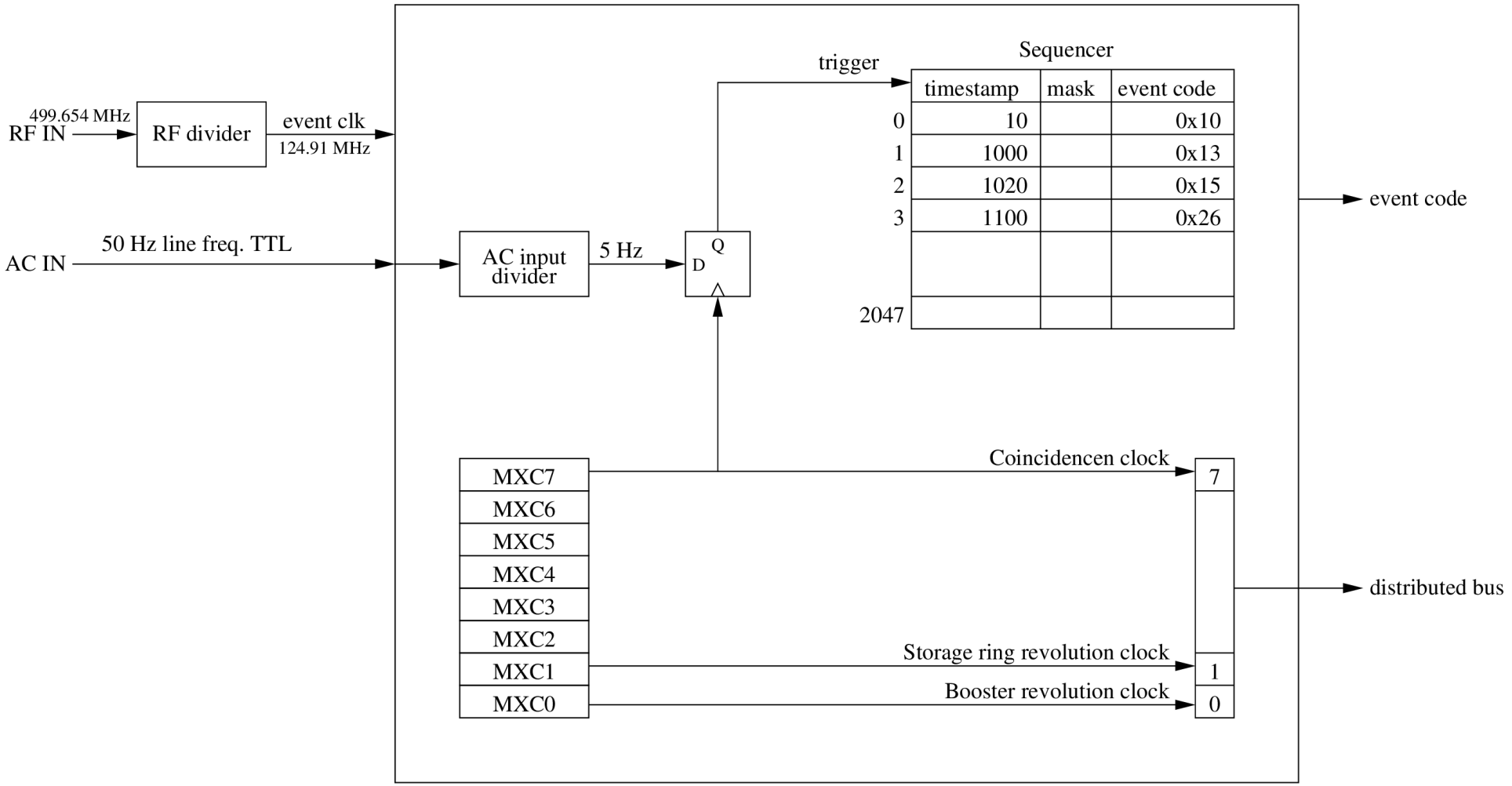
EVM configured as System Master



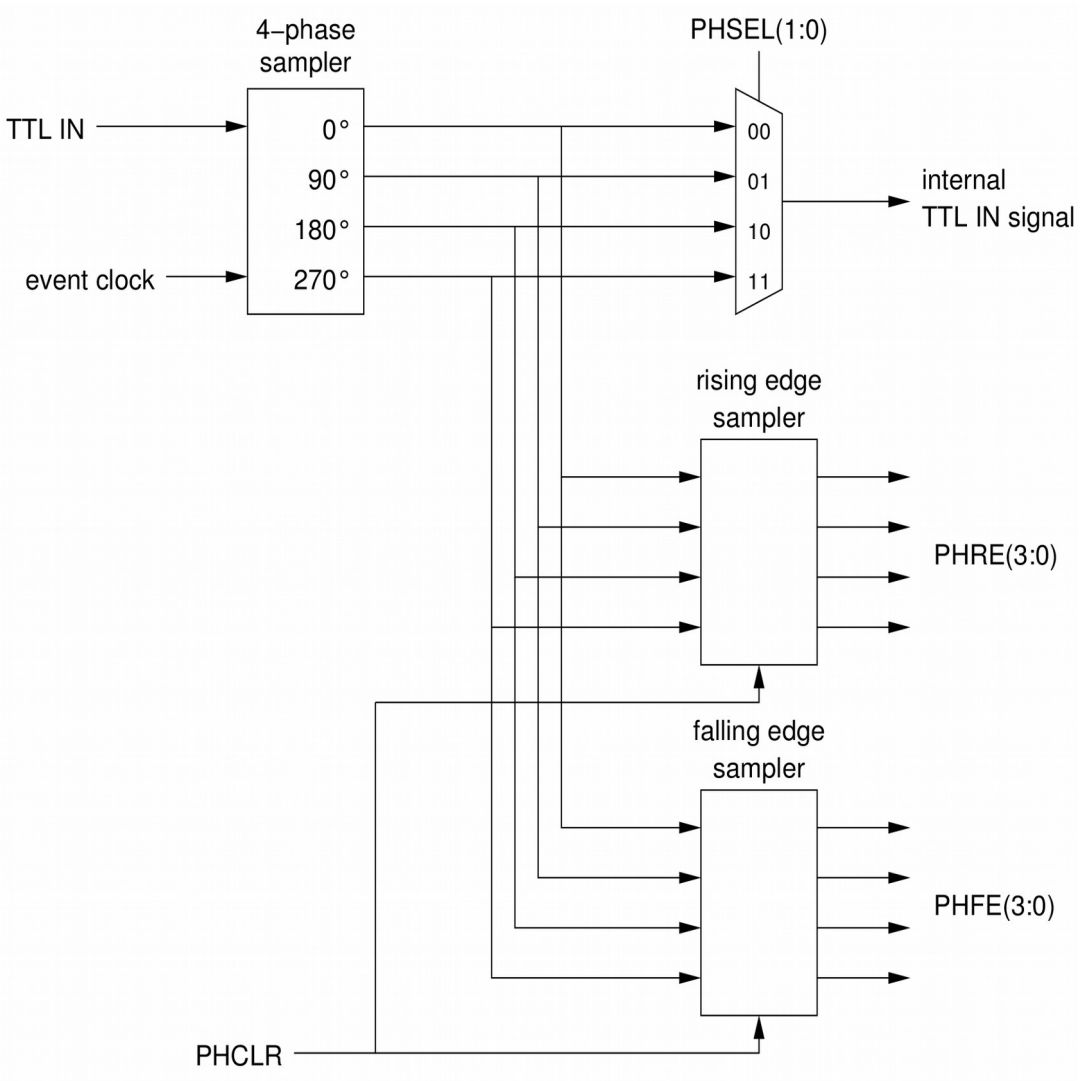
EVM configured as Fan-Out



EVG Example for Synchrotron



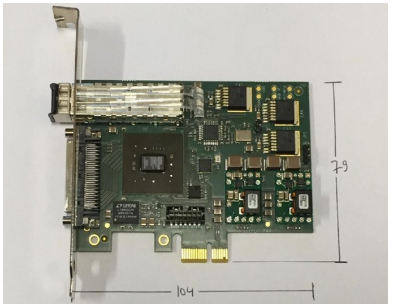
EVM Front Panel TTL Inputs with Phase Select and Phase Monitoring



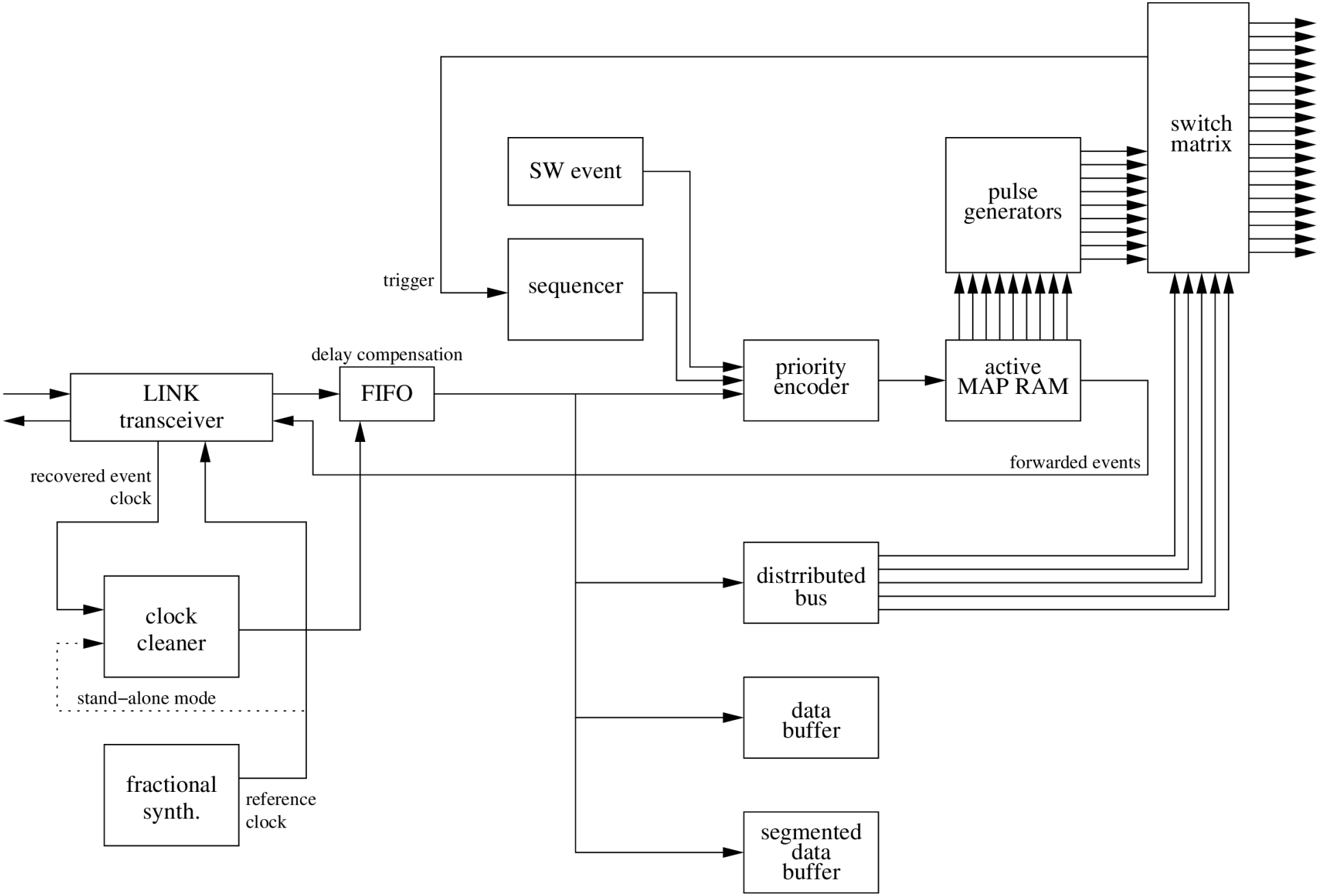
- Allows using externally generated subharmonics of the event clock for e.g. triggering sequencers
- Due to data transfers the distributed bus in running at half rate (event clock/2), logic has been added to be able to match the distributed bus phase with the rising edge of an external signal
- Use case SwissFEL: superperiod generated externally

Delay Compensation EVR (VME-EVR-300, mTCA-EVR-300, PCIe-EVR-300DC)

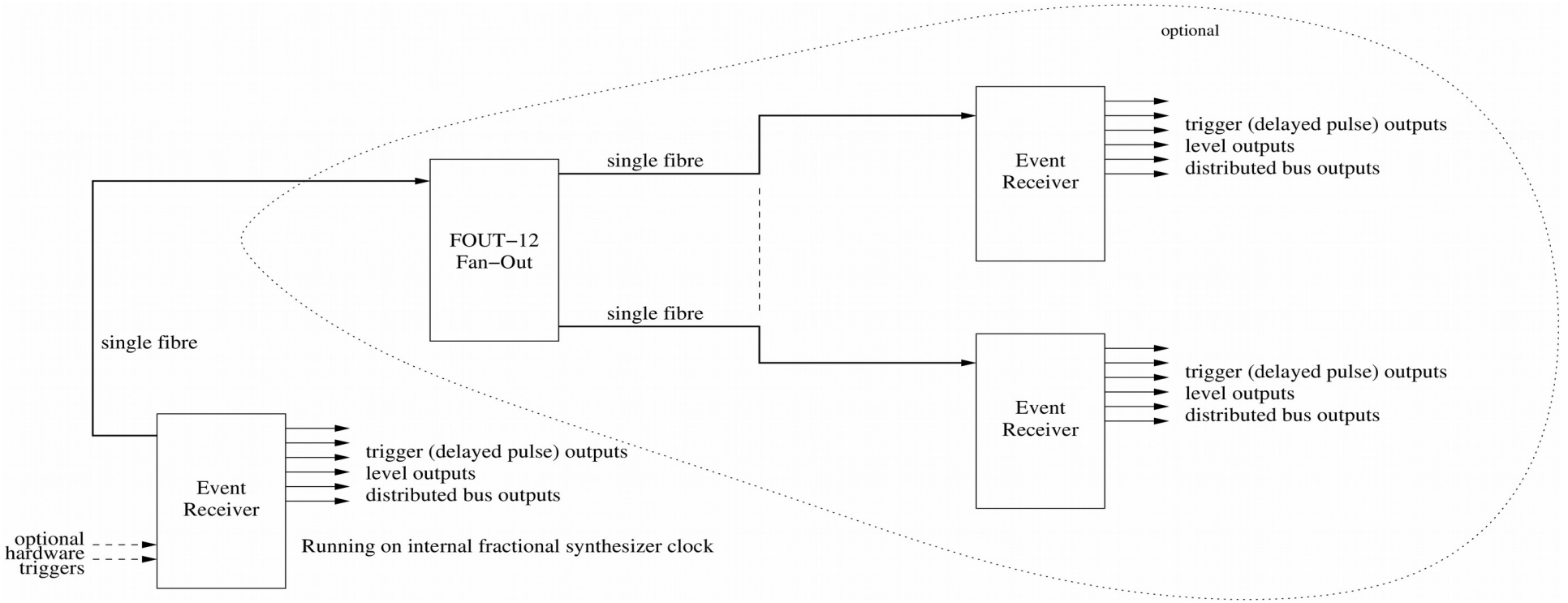
- Stand-alone operation without EVG running on internal reference clock
- One Sequencer similar to EVG sequencer
  - Can be triggered from pulse generator output (event) / distributed bus bit or prescaler output
- Software events
- Can be used in both DC and non-DC mode



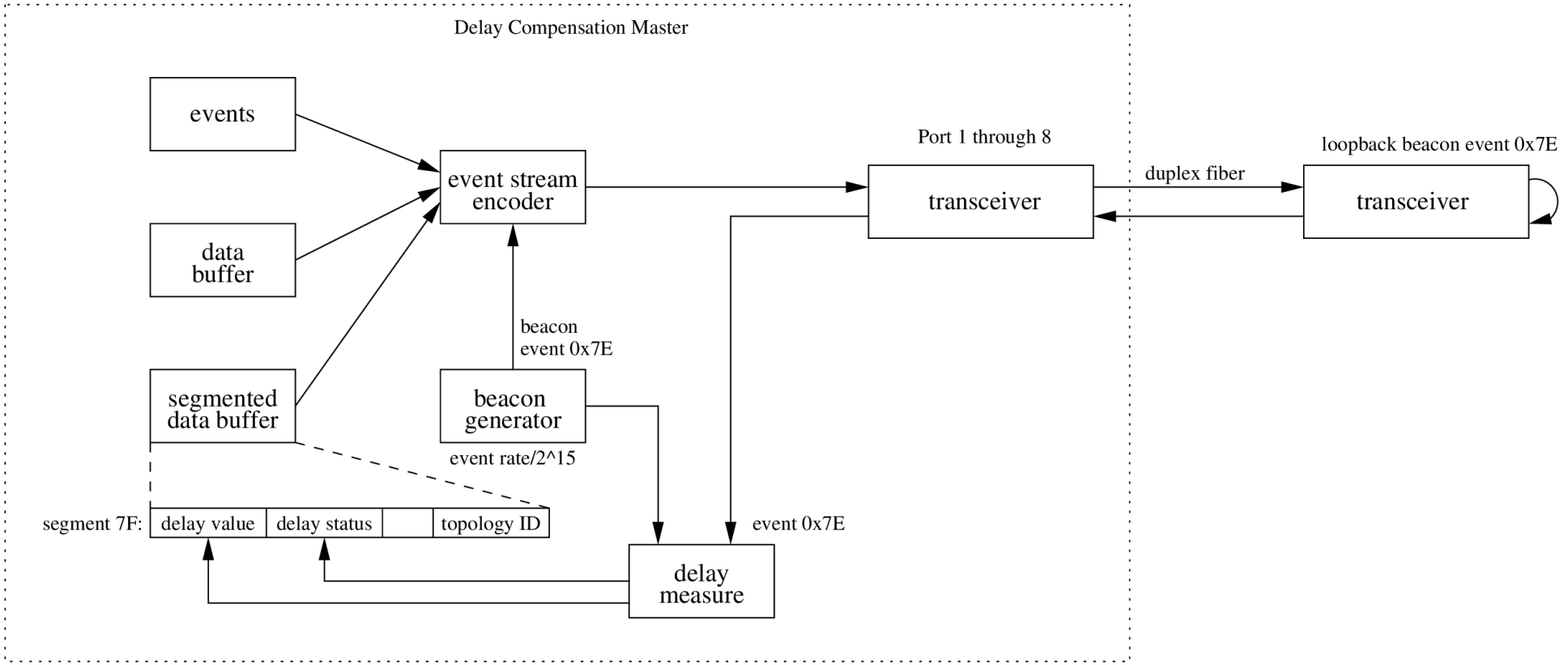
EVR Simplified Block Diagram



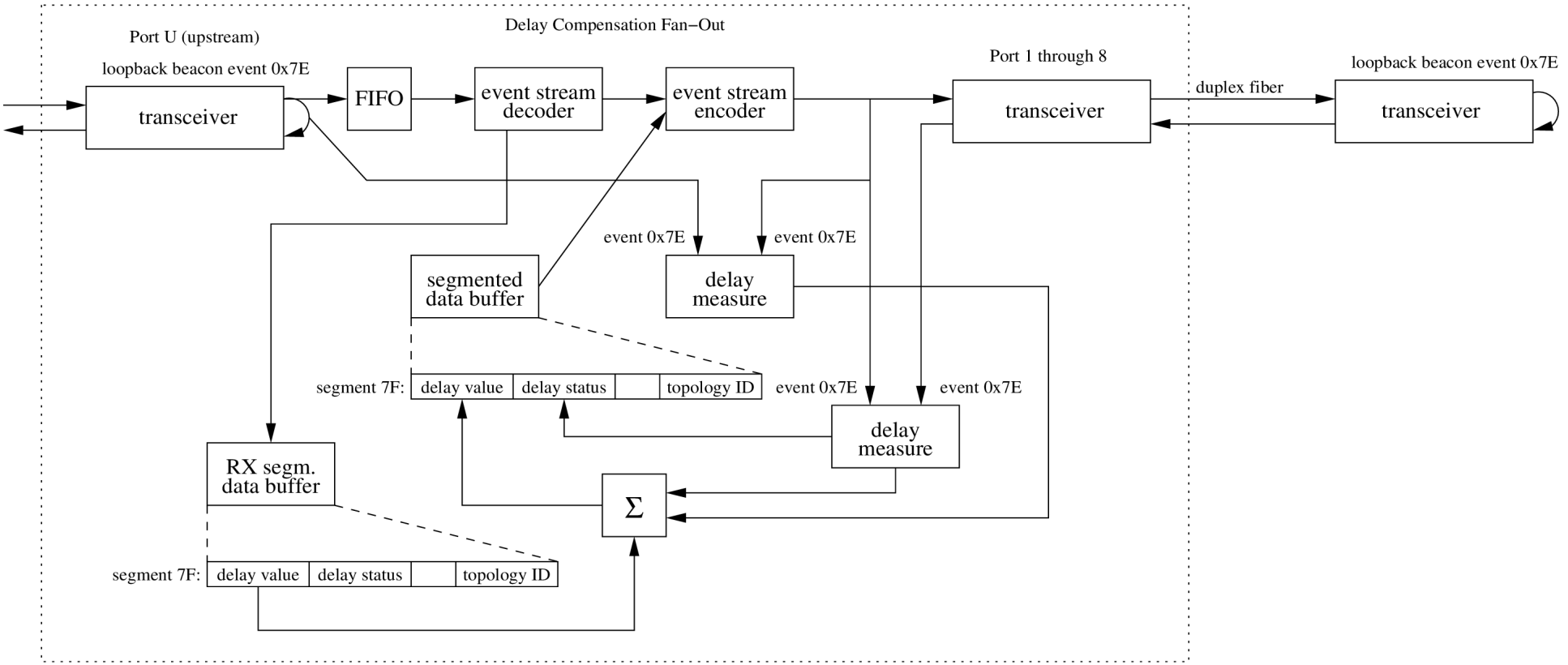
Simple System without EVG



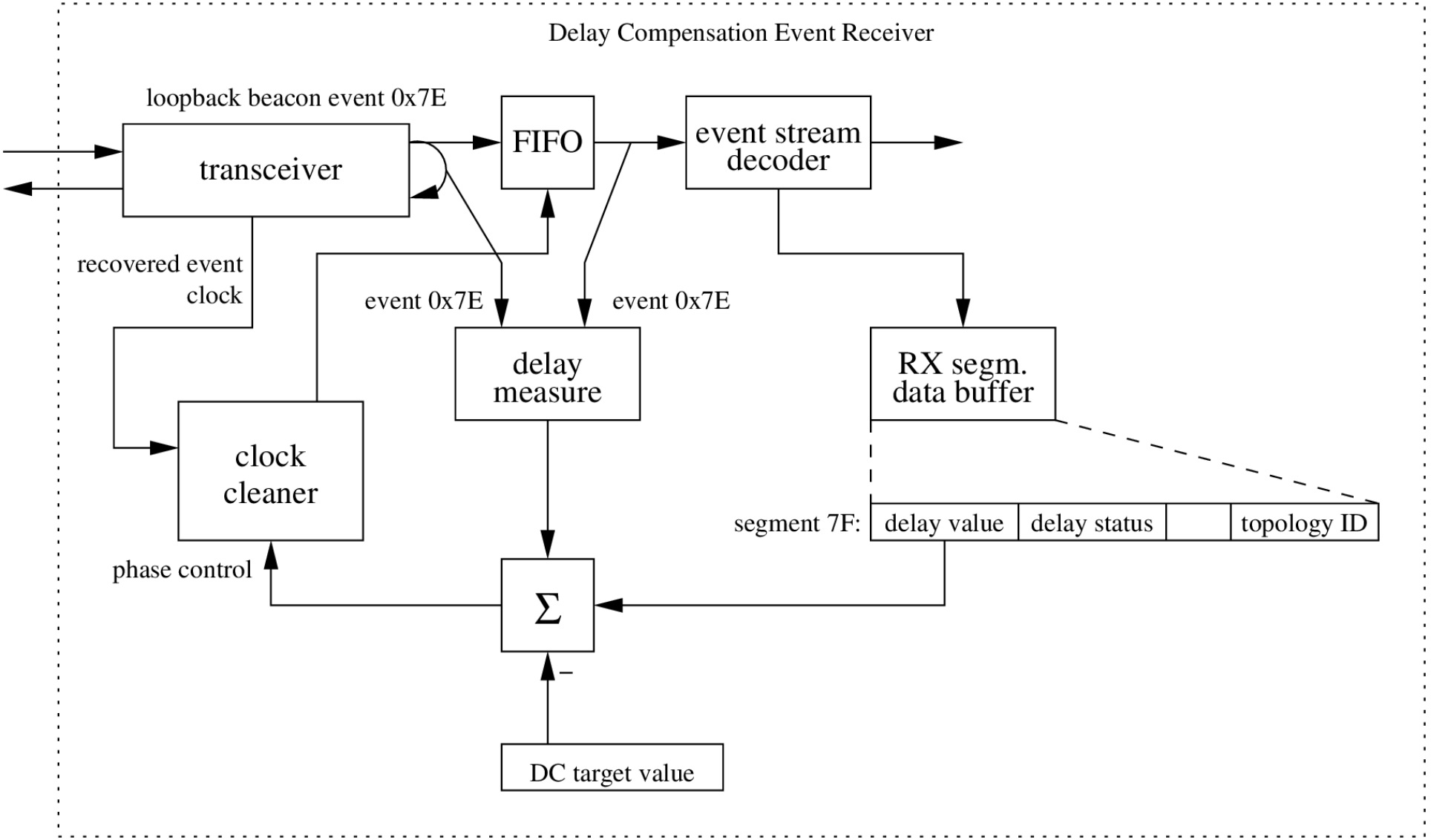
VME-EVM-300 Configured as Delay Compensation Master



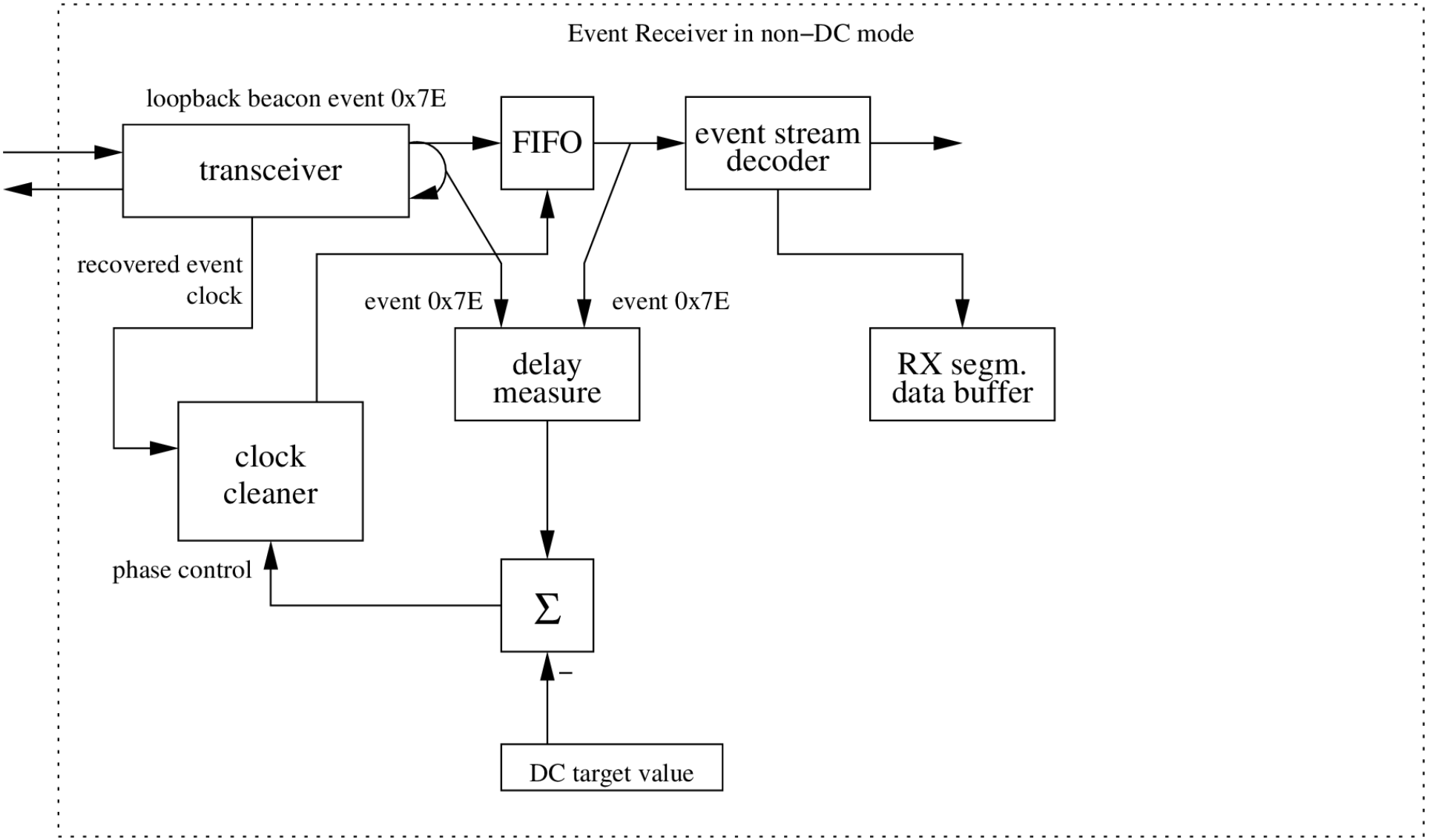
VME-EVM-300 Configured as Delay Compensation Fan-Out



Delay Compensation Event Receiver



Non-Delay Compensation Event Receiver



Compatibility with the Earlier Protocol

- Delay Compensation extends the protocol by:
  - Using event code 0x7E as beacon event
  - Adds the segmented data buffer that uses a different transfer start “comma character” than the data buffer
- Both protocol changes are ignored by pre-DC event hardware
- Timing is similarly deterministic as with a pre-DC distribution network
- Delay Compensation EVRs can be used with the earlier protocol in non-DC mode
  - The Delay Compensation FIFO can be used to fine tune the EVR output delays as a group with very high resolution

- EVMs require the top node to be configured as the Delay Compensation Master
- EVMs can be used in Delay Compensation Mode only